APPLICATION NOTE:

EMC BEST PRACTICES - PART II

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EXECUTIVE SUMMARY

Part 1 featured the skin and reverse proximity effects that develop due to electromagnetic field action in and around conductors. Several themes were declared. In the final part of this application note, examples are used to illustrate a few good EMC (electromagnetic compatibility) practices.

MARKERS FOR NAVIGATING TOWARD THE GOAL OF EMC

Frequency Domain

Understanding what is to be achieved sets the right expectations when it comes to quelling EMI (electromagnetic interference). We know that EMI consists of a mix of CE (conducted emissions) and RE (radiated emissions). To give an idea of the relative difficulties involved, consider the amount of bandwidth that is surveyed during assessments for noise energy accumulated across the frequency domain. For CE, expect anything from 150 kHz to 30 MHz – for RE, we can expect a design to be assessed in the bandwidth extending from 30 MHz to 1 GHz - 5 GHz or more – clearly a much larger bandwidth than for CE.

For CE, the focus is mostly on circuits and how they are embodied in substrates, which support traces that connect mounted components. When it comes to handling RE, a successful design that has CE countermeasures built in is easier to manage as we consider how to protect those assemblies against RE.

Conductors define the launch and landing points for EM fields that couple with them. The resulting RF antenna exhibits an indiscriminate capability of transmitting and receiving EM energy – transporting noise to and from loops that match the dimensions of part of, or several wavelengths of the EM field. The wavelength of the frequency content of the field is defined by c = f.,□ where c is the speed of light [ms-1], f is the frequency [Hz], and □ λ is the wavelength [m]. Be aware that these unwanted energy transfers may involve resonances in specific parts of the frequency spectrum. It should come as no surprise that a large proportion of EMI stems from the cabling configuration used for connecting boards or long traces within a PCB (printed circuit board).

Signaling Impedance

When a digital data-processing circuit is affected by emissions coupling into it, it is said to be experiencing crosstalk. In the digital world, the use of noise margins and error-correction encoding tends to limit problems in all but the most severe environments. In the analog world, there are no guard rails: If we take transducer signaling in general, it tends to be of low amplitude, presented from a high impedance source. Impose emissions on such weak signals, and the ability to interpret

the valuable information is lost. Buffering is the process that replicates the same signal's information content, transferring it into a low impedance output circuit. It is often combined with a filtering action. Current signaling (such as the 4-20 mA current loop protocol) in a low impedance circuit is less sensitive to noise. This protocol fills a niche for remote operation in noisy electrical climes.

APPLICATION SURVEY

Partitioning A System For EMC

Sources of EMI originate from hard switching operations or fast electrical transients, which are either present in the application or imposed externally. It is essential to identify circuits that may generate or accumulate these stray energy flows and then work to contain them.

We are used to seeing electronics in enclosures. At first sight, a box with controls, indicators, and external connectors facilitates human interaction, whilst separating the electronics from the operator. It also permits robust and consistent operation. Good EMC development deals with the application as it is physically constructed within such an enclosure; there may be just one or several printed circuit assemblies and their interconnect. Scoping out a system, we might observe other collections of electronic substrates within their own separate enclosures that are installations within a larger cabinet, rack, or framework.

Good EMC evolves from this management of complexity through partitioning – each module can be designed and defended against both its self-induced and external noise sources. The enclosure is a boundary - anything that goes through it needs some interface: for example, combinations of shielded cabling, a filter stage, a buffer amplifier, or driver.

The partition defined by the enclosure should physically be as close as possible to a 3-dimensional, continuous conductive surface that acts as an electrical shield, blocking or reducing RE. If we are dealing with, for example, a steel box, this would be a six-sided shape - the application ultimately must dictate the best geometry and conductive material for the chosen enclosure.

Clearly, any gaps (whether they are necessary or not) or poorly bonded / non-overlapped seams that constitute openings in the casing invite radiated EMI as the dimensions of the physical gap approach a fraction of the wavelength of an emission. Even a hairline crack poses issues. Eddy currents induced by RE can move from, e.g., an internal surface of the enclosure to its outer surface (recall skin effect). The edges of the gap widen the loop around which these eddies must flow, and at the right frequency, the EM waves start to move through it into the surroundings. A rule of thumb to adopt is to ensure that no gap exceeds a dimension of [□ /10] of the highest frequency content of the RE – at 1 GHz, this dimension works out to be 3 cm. Conductive glass panels for indicators and metallic grills for shielded airflow must be firmly bonded to the metal enclosure, helping prevent significant loss of shielding in these situations. There are many preformed miniature shield boxes, coatings, and conductive films that are available that can absorb radiated energy. These can be

applied to parts, particularly high-speed ICs, as well as the surfaces of a non-conductive enclosure. Local EM field containment is mandated.

The reader would now appreciate the folly of establishing a zero-volt return link by connecting a ground plane on a single board that might be one of many inside a module enclosure directly to the system's chassis, bypassing the enclosure shield - violating this EMI confinement principle. This pathway, likely being long, adds a lot of parasitic inductance, which defeats the original purpose for which it was intended, resulting in an inadvertent antenna.

The way components are situated in relation to each other on a PCB can either enhance or mitigate the deleterious effects of noise. Configuration of a board assembly based on good EMC principles will improve the board's performance without significantly changing its cost.

The directed effort involved in adopting correct board layer stack-up, component placement, trace routing, and grounding is not much different from that which would be expended in producing an unusable PCB assembly. Correct EMC implementation also improves the circuitry's ability to operate in the presence of noise, reducing its susceptibility to it.

Recurrent Issues

Clock, strobe, and associated distribution networks, digital control signaling, lower-order address and data bit lines, and their drivers, motor control, and SMPS (switched mode power supply) circuits tend to be the dominant sources of noise within an application.

Transients may cause fleeting, hard-to-track issues manifested as loss of communication/control or data. Lightning, AC power disturbances, or harmonics from the utility may cause these electrically fast events.

Besides power switching devices in SMPS, electronically controlled motors and heaters, luminaires, and low power lighting – all exhibit extremely high rates of dV/dt and dI/dt, which produce wideband RF emissions. Unlike the steady clocks synchronizing digital operations, SMPS modules may work differently when the load changes, for example, going into pulse-skipping or hysteretic mode in standby or low power operation. Such SMPSs have noise signatures containing spurii that walk up and down in the frequency domain between operational modes. Clearly, all aspects of the operation of SMPS must be known so that adequate EMC measures can be applied.

ONE BAD AND ONE GOOD EMC PRACTICE

I hinted in part 1 that identifying *parasitics* associated with coupling between circuit nodes is something we can do with the help of schematics.

Star-Point Grounding: The Worst Loop In the World

A star-point ground is conventionally used to draw together separate ground return wires or traces, fixing them to a common zero-volt reference node. Figure 1 shows a system that incorporates three

functional blocks on a PCB. The idea behind star-point grounding illustrated here is that it addresses a concern that any disturbance in the current from a power rail being fed downstream along a single return conductor shared by all 3 PCBs is likely to change the voltage being sourced upstream due to the voltage drop changing in the *daisy-chained* return conductor.

The primary issue with this method is that large loops are formed in the power network. Each of these loops will receive or generate radiated EMI, which can interact adversely with the other circuit loops.

An equivalent circuit of this star-point system is shown in Figure 2. Inbound power and the return conductors are used to model the electrical behavior of the loops interacting with H-fields. Note that signal currents are sourced and returned via the power supply. Including E-field coupling would necessitate the inclusion of parasitic capacitors.

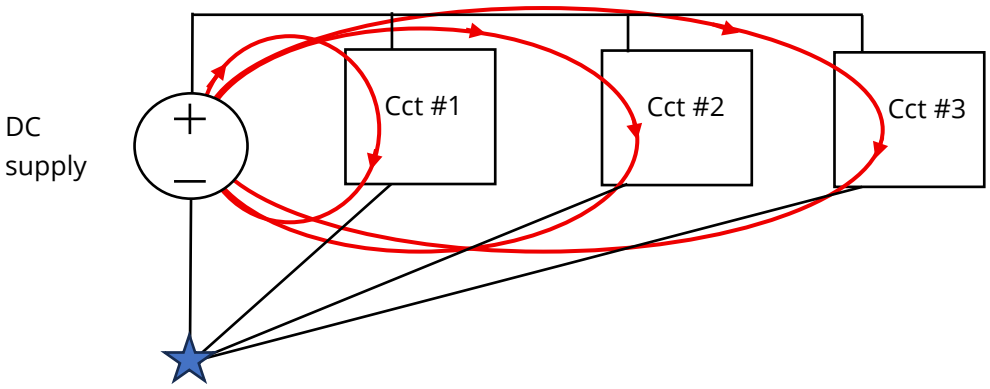


Figure 1 – Star (single)-point grounded DC power supply servicing three functional blocks on a single board assembly. The return power conductors have been separated, resulting in large loops that can deliver and pick up EMI.

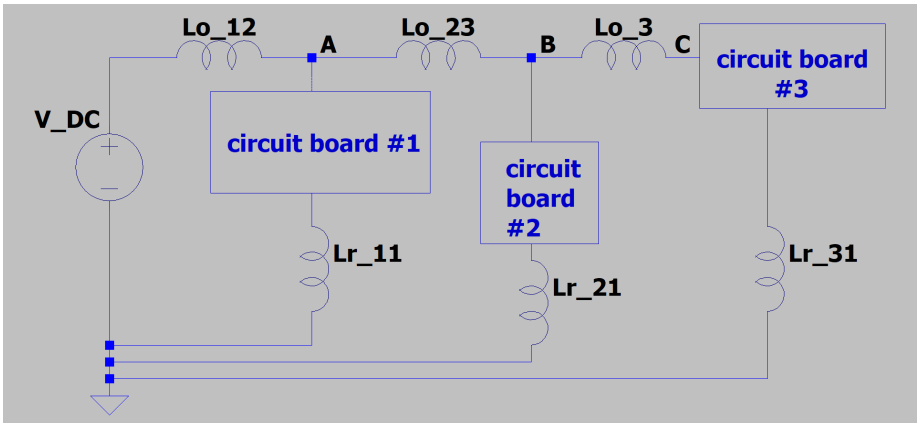


Figure 2 – approximate lumped element equivalent circuit schematic of a star-grounded system

Each of the inductances illustrated in Figure 2 will be different. I try to break with the uniform representation of a schematic to emphasize that the circuit boards will be in various positions within their assigned enclosure, with varying distances between themselves as well as the returns and the star ground. A better representation of the conductors connecting the circuits would involve replacing each inductance with the T-equivalent circuit shown in Figure 3 to accommodate EM coupling in the individual traces.[1] A star-point ground clearly hinders EMC.

You may ask the question, "Inductance and capacitance of interconnects are unavoidable, so how can they be dealt with?" We know that small, tightly coupled loops confine EM fields effectively. If a trace is widened over a dielectric ground plane structure, this reduces its inductance whilst making its capacitance bigger. This makes the trace impedance lower according to the equation $Zo = \sqrt{\frac{Lc}{Cc}}$ where Zo is the characteristic impedance of the trace [ohms], **Lc** is inductance [Henrys] and **Cc** is capacitance [Farads]. All signal lines should have a fixed impedance. Aim for the lowest impedance consistent with generous allocations of copper to power traces by making them thick (for the DC ampacity) and wide for low impedance.

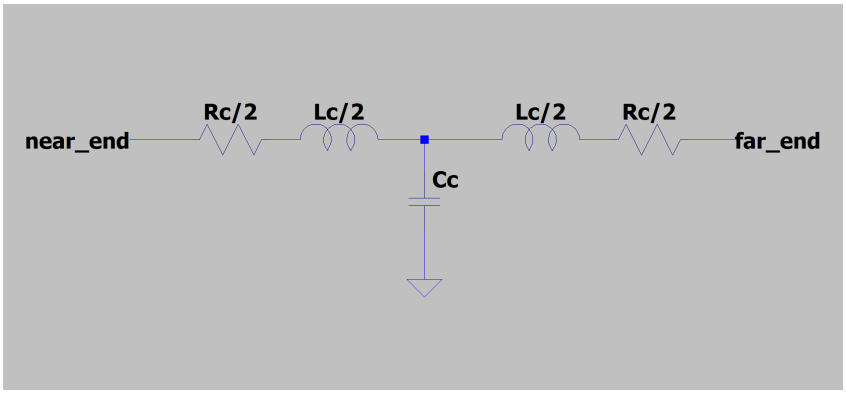


Figure 3 – distributed element equivalent circuit for a single conductor. C is the capacitance, R is the resistance, and L is the inductance per unit length of conductor.

Antidote to Star or Single-Point Grounding

Tight conductor pairing – When connecting a DC lab power supply to an application board using insulated in-bound and return (so-called "red" and "black") wires, these are often twisted together to minimize power supply loop size: TWP (twisted wire pair) reduces loop inductance; The twists result in regular, reversed orientation of the positive and negative lines, minimizing the effects of EM fields

[1] Consider {traces, conductors} as well as {circuit boards & substrates} synonymous

interacting with these conductors[2]. It also tends to result in a more consistent impedance. TWP, with matched outbound and return conductors, is the electrical equivalent of setting traces over a continuous ground plane on a printed circuit board. Figure 4 shows an approach that uses small conducting loops for both intra-PCB and between modules making up a bigger system.

The reader will notice that local power decoupling capacitors are featured, set close to the signal processing elements within each circuit module, providing a short bypass path to the ground return. These capacitors act as charge reservoirs for local dynamic current delivery to hold the DC voltage constant during signal processing or switching operations. The selection and placement of these capacitors calls for minimal ESL (capacitor inductance), connected using the shortest available trace. Keeping the inductive decoupling parasitic to a minimum improves suppression of wideband noise. It was mentioned that widening any trace for a given separation makes for a lower impedance interconnection. The ground return conductor is swapped for what is termed a GRP (ground return plane).

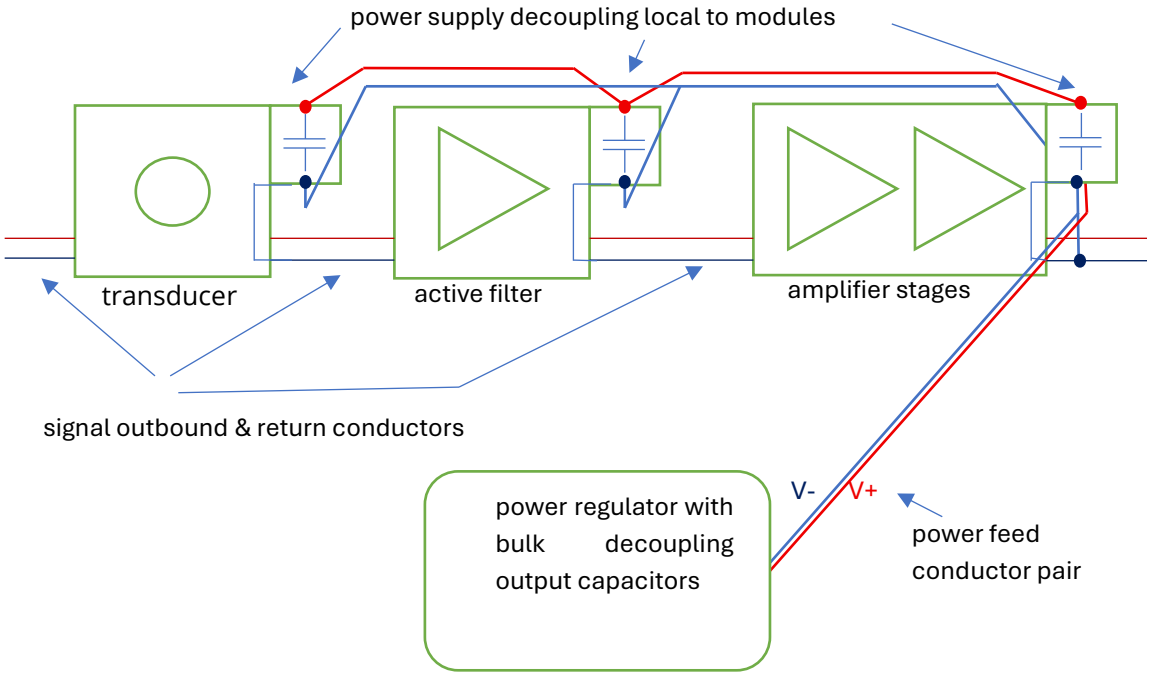


Figure 4 – EMC-oriented block diagram of 3 functional blocks on a PCB showing signal and one of several power rails being routed over a circuit board

[2] Exceptions to using twisted pairs on the bench include hi-pot and high DCR (DC resistance) testing

SOME MORE GOOD EMC PRACTICES

Four additional EMC measures are highlighted – cable shielding, differential buffering, placement of {X,Y} caps, along with other special discrete components, and board stack-up design.

Cable shielding and termination

We have already seen the benefit of dedicated conductor pairs with small loops: CM noise can be reduced further by using STP (shielded twisted pair). STP is manufactured by adding a thin metallic foil wrap over individual TWPs. The foil should be complemented with an outer wire braid, over which goes a jacket of insulation – a multiconductor composition is shown in Figure 5. The conductive shield layer, when exposed to an EM field, will reflect, absorb, and redirect its energy - just like a conductive enclosure. It is essential to connect the shield uniformly around its circumference to the enclosures at each end so that the cable's impedance remains uniform. Such terminations of the shield at both the near and far ends are mandated – pigtails or thin wires connecting between the shield of the STP or coaxial cable present unwanted inductance.

Differential signaling

A weak signal is easily impaired by noise, so it is necessary to provide a buffer, effectively increasing its current without distorting it. This can be done with a combination of single-ended amplifier and low-pass filter stages. Achieving filtering in the presence of wideband noise will still leave noise within the usable passband of the filter, degrading signal integrity. Most filters tend to suffer *regeneration* – loss of attenuation at frequencies above the stop-band, which will add noise back onto the signal.

Figure 5 – multiconductor STP example with 4 STPs, wrapped with conductive mylar, outer shield, reinforcing metal braid, and insulating jacket

We need to carry signal **Vs** through our application with the lowest noise. It will be applied differentially, i.e., across 2 conductors, neither of which is referenced to zero volts.

Before noise is introduced, $Vs = Vr - Vb$ the potential difference between individual conductors **r** and **b**. As the signal courses along the conductors, CM noise **Vn** is injected into each conductor, voltages of which become **Vr'** and **Vb'**

$$Vr' = Vr + Vn$$

$$Vb' = Vb + Vn$$

A differential amplifier will provide the signal it observes *between* its input terminals, with a gain **G**.

$$Vout = G.(Vr' - Vb')$$

$$Vout = G.([Vr + Vn] - [Vb + Vn])$$

$$Vout = G.(Vr - Vb)$$

The theory tells us that CM noise is eliminated whilst the proper signal gets amplified. We still get to lose CM noise with differential signaling alone (with **G** = 1).

Signals leaving or entering boards and enclosures should be processed using differential signaling, as shown in Figure 6. Electrically long traces, i.e., with physical length > [□ /10] on a board, also benefit from being treated in this way. Note that the system enclosure or other so-called *structure* (chassis, cable tray, rack, frame) circulates common mode currents; it should never carry power or signal return currents. An implication of the nature of the signal flow of Figure 6 is that there is minimal coupling between the output and the input. Cabling assemblies should be arranged to carry signals in direct, rather than in serpentine or meandering routes around modules or circuit boards within enclosures.

Figure 7 shows LTSpice™ modeling and outcomes that demonstrate analog or digital signal differential buffering in the presence of noise induced in a matched conductor pair.

H- and E-field coupling is modelled separately using parasitic inductance and capacitance. The fields might be due to closely spaced traces (near field) or coming from remote sources (far field). The reader will notice that the signal wires are no longer externally referenced. In an STP scheme, the shield of the cable is connected to a GRP. GRPs should be solid shapes with no slots or long gaps; otherwise, with such discontinuities, there is the possibility of producing RE, as the return current finds a sneak path to close a loop of indeterminate length and links via EM fields to other circuits nearby.

If there is some difference in the conducting paths in the signal wires, then the CM noise converts into DM (differential mode) noise, and this noise will be added to the processed signal. The reader is invited to alter the coupling between the inductors or the relative values of coupling capacitance slightly to see the effect of this imbalance.

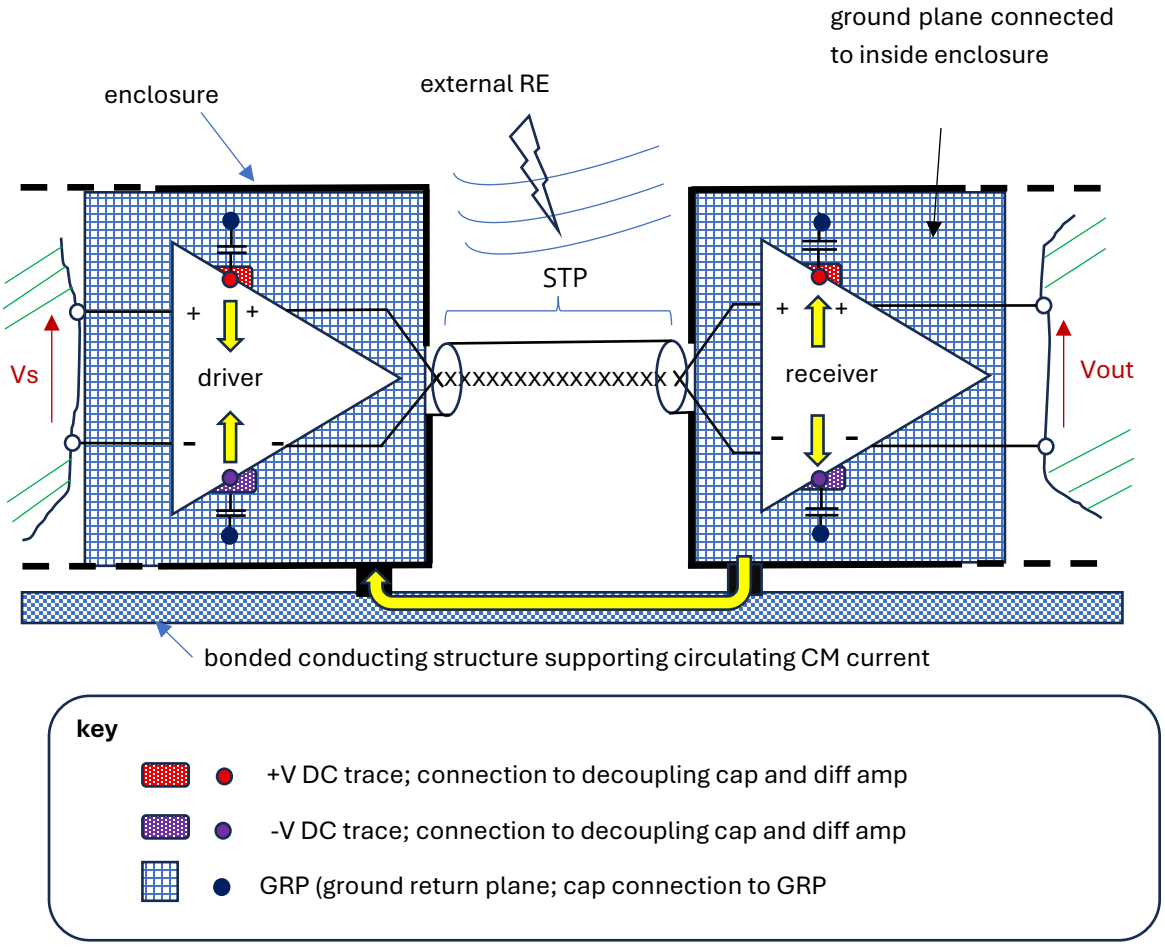
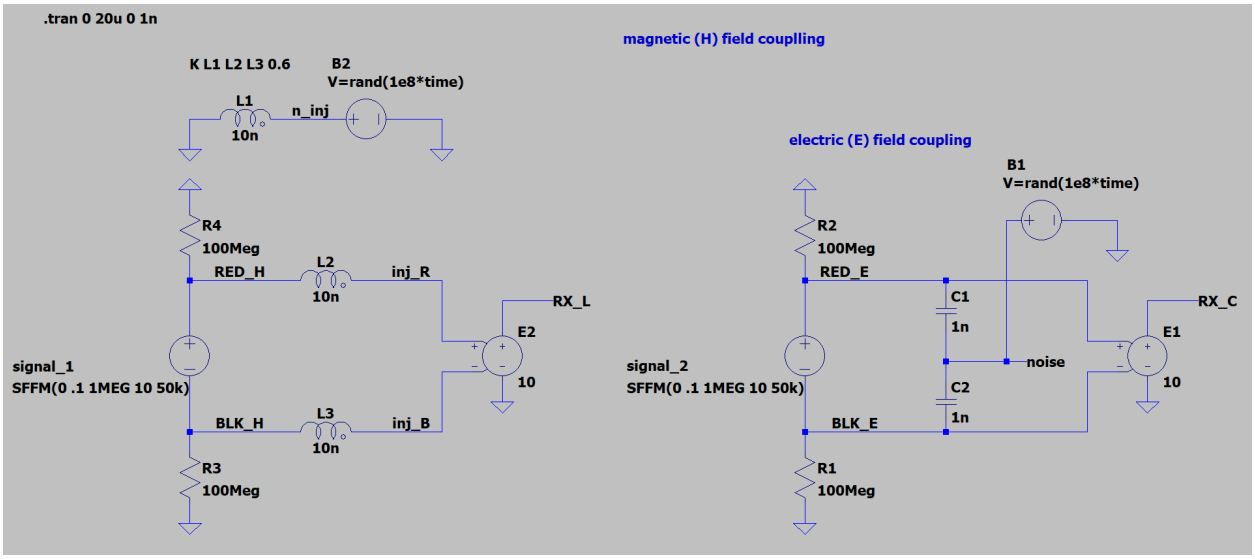
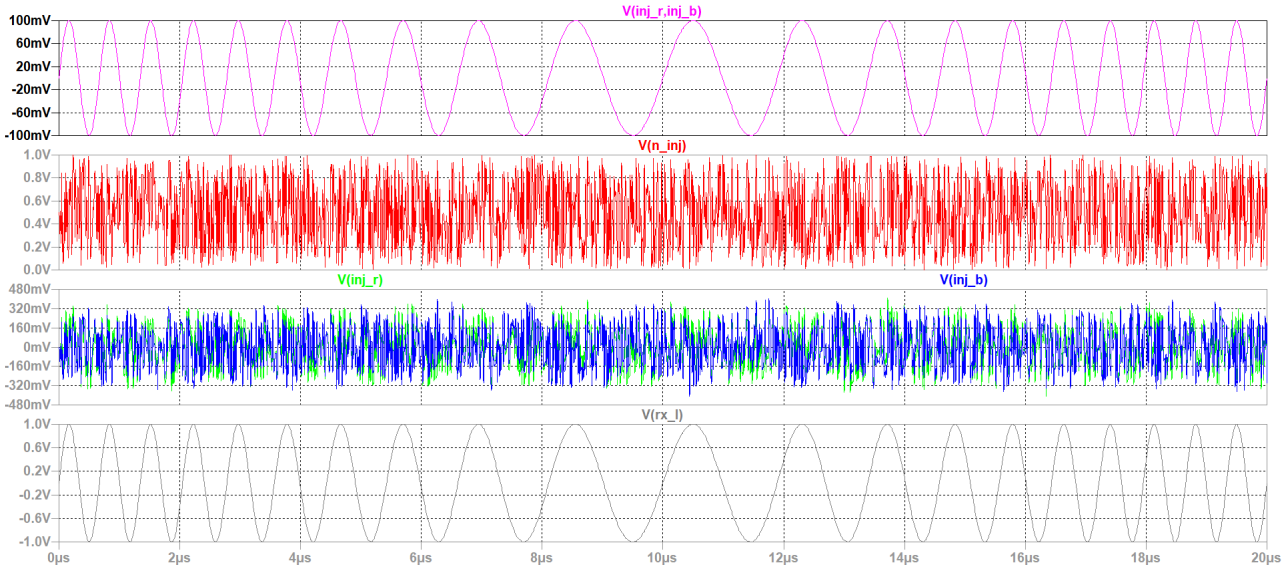


Figure 6 – differential signaling showing some of the many CM current pathways



(a) differential signaling time domain simulation in LTSpice



(b) Waveforms associated with H-field CM noise simulated with coupled inductors. Cyan trace is the useful signal - a frequency modulated sinewave; Red trace shows the noise source - a random noise signal with 1V pk amplitude. Green and blue traces show the signal lost in noise within inbound and return conductors. The output signal – purple trace – emerges from the differential gain stage, cleared of CM noise.

Figure 7 - Differential signaling helps to remove common-mode noise induced in signal-carrying conductors, shown for the H-field CM noise case.

Use of Passives and Modular EMI Filters

SMPS have been identified as significant sources of noise: Various means are used internally to close fast current loops using RCD (resistor capacitor diode) snubbers to good effect, set around power switching elements. This is a detail to be found in other treatments. Even so, there is still CM and DM noise to contend with from these and other systems previously mentioned. Filtering out noise produced by these *power oscillators* involves either blocking high-frequency currents or letting them bypass the defended circuit altogether. The most economical option is to use appropriately rated passive components: Inductors for blocking and capacitors for bypass functions. Ferrites can be likened to frequency-dependent resistors, absorbing or dissipating energy most effectively within specific ranges of frequency. To make a lossy inductor or capacitor would involve adding a resistor in series or parallel with it.

Inductors used in power filters should have saturation ratings that are greater than the maximum current they may need to deliver. Capacitor selection involves being selective about the structure as well as the rated voltage and the amount of frequency-dependent capacitance available. Some vendors offer impedance vs frequency plots to help with assessing the suitability of a given component.

X- and Y-caps, deployed close to power switchers, are constructed to minimize any possibility of failing and turning into short circuit paths. This robust behavior is specified as a pulse rating. Both these safety-rated capacitor types have internal resistance, defined as ESR (estimated series resistance). The presence of any resistance in a passive tends to dissipate energy from noise current sources or damp out oscillations caused by transient disturbances.

It may be the case that several stages of filtering are needed. Good EMC designs will have a particular arrangement: higher frequency countermeasures are deployed within the immediate area where the DC/DC converter is situated on a supporting substrate over a GRP to which the Y-caps get terminated, with outer layers of the defense using components that tend to have better low-frequency attenuation characteristics.

Figure 8 shows an example of how such measures might be contrived around a power switching module. Note that *line filters* come in their own casing. The use of a line filter, depicted as an input EMI filter module in Figure 8, must be electrically bonded and grounded to the conductive enclosure.

This filter may provide some degree of transient and lightning protection, but this likely requires augmentation. Single or combinations of MOVs (metal-oxide varistors) and TVSs (transient voltage suppressors) work in conjunction with ferrites in this example to dilate peak transient energy levels to acceptable levels over time. MOVs have high energy standoff capability, whilst the TVS clamps and holds the peak voltage of a transient to an acceptable level. Ferrites are frequently added to power cabling, a measure omitted from Figure 8.

Such component additions can be used to reduce the effects of noise coming from any particular module identified as a noise source, besides SMPS units. The SMPS output power port is not shown, but the reader should understand the need to place X and Y caps closest to the SMPS, followed by filtering stages thereafter.

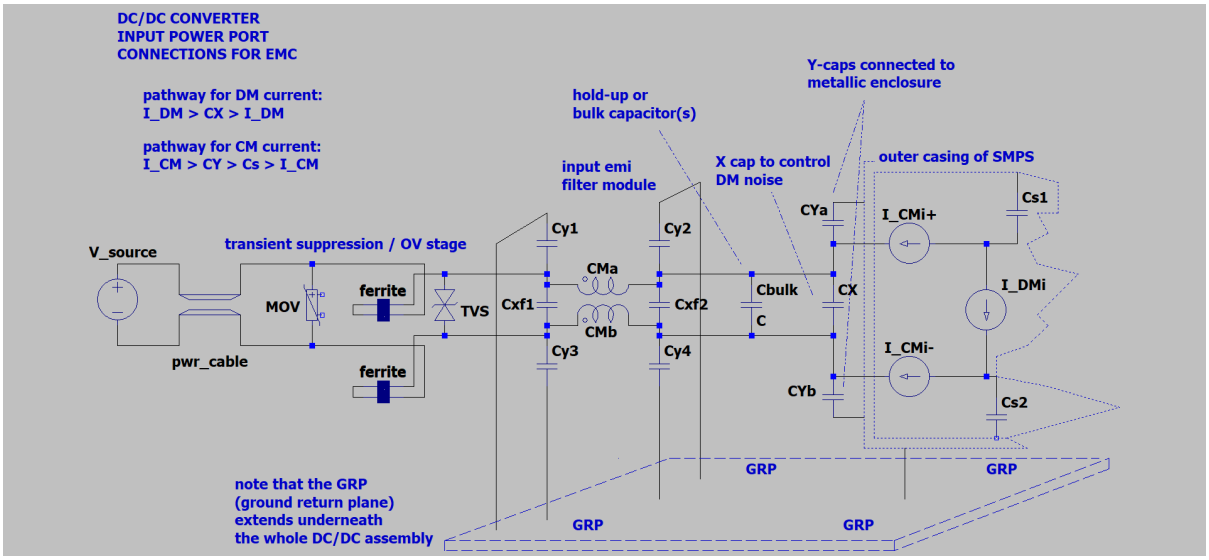


Figure 8 – showing EMC measures applied to the input section of a DC/DC converter module

Board Stackup Design

Figure 9 shows a cross-section through a PCB showing alternating layers of copper and insulating substrate material. The signal/power routing copper layers are machined or etched to form the traces for connecting signaling and power components. Areas between large traces should have *pours* (larger areas of conducting material) applied for grounding, so arranged in between traces to reduce crosstalk between them. GRPs are formed out of a whole copper layer for a signal or power to be referenced to. The core section - consisting of a cured dielectric with dual copper facings - is the foundation on both of the PCB's sides for additional layers of pre-impregnated substrate material (e.g., fiber glass impregnated with a resin) to be deposited on and then sheathed with yet more copper plating. The outcome is a sandwich of alternating dielectric and metallic layers.

Notice that the GRPs are always set immediately adjacent to the signal and power routing layers. In contrast, if several signal/power routing layers are set in between GRPs, then the ability to control EMI will fail as some of those layers are not directly referenced to a local GRP.

EMC needs to be considered in both the vertical and 2-dimensional planes for each layer. Via constructions provide vertical connections through the PCB stack-up to connect a trace in one part of the stack-up to another trace in a different layer (see examples of some via types in Figure 10). These

are used to reduce board area – the designer can save space, but at the cost of adding parasitic inductance. *Via stitching* is the placement of several parallel vias arranged as a matrix to form a lower inductance connection. This is used to connect GRPs within the different parts of the stackup together. Most board stackups involve the use of several signal/power and dedicated GRP pairs. The use of vias for stitching GRPs together around the circumference of the board prevents the launch of radiation from the board's edges between GRPs from internal traces used for high-speed clock and digital signaling. The reader will notice such stitching in the copper pour in the top section of Figure 10.

The three larger vias forming a line along the right side of the picture are plated through, providing additional conductance between the pour and the GRP. Signal traces going through the pour have controlled impedance characteristics. Pads can be seen onto which components are to be connected. The matrix of vias along the top right corner of the picture permits sinking of heat from an element to cooler layers within or on the outer part of the stackup.

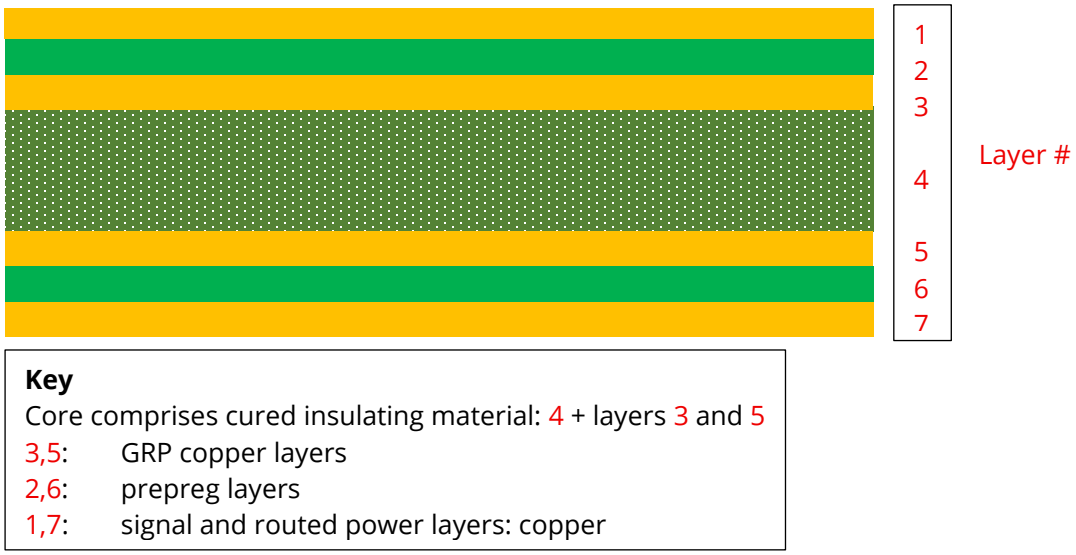


Figure 9 – Cross-section of a 4-layer example board stack-up for EMC

Test points are often provided on the PCB with the good intention of easing the process of verifying circuits – opt for impedance-controlled arrangements using either Johnson Jacks or more refined RF SMT coaxial structures. Any test pin on a PCB otherwise acts as an antenna.

Board Connectors for power and I/O (input/output signal connection) should be bonded to GRP and aligned along a single edge of a board assembly, located away from fast clock and signaling lines.

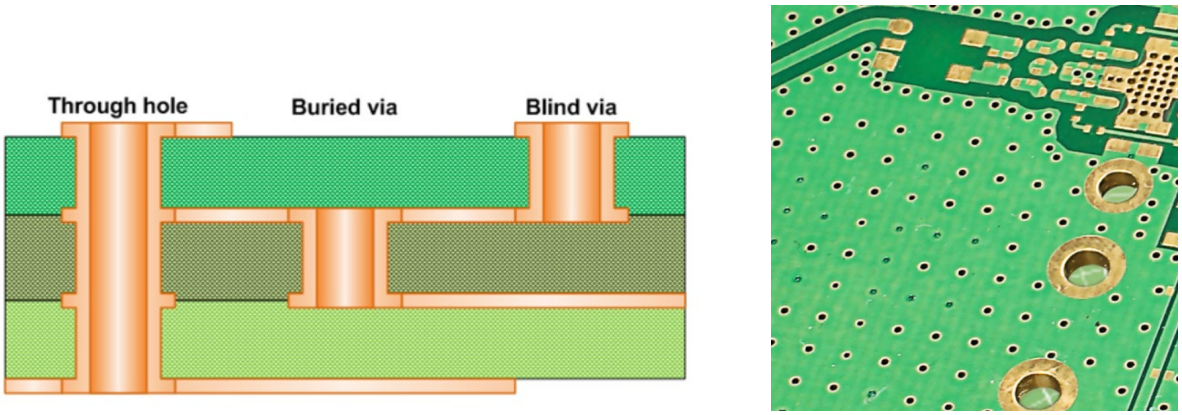


Figure 10 – Circuit board cutaway and top views showing several different types of VIA[3]

CONCLUSIONS

EMC best practices are continually evolving to keep up with systems that utilize fast, low-loss switching as well as with aggressors that emit external EMI. Some of the foundations of the approach are embodied in a small number of techniques highlighted in this article. They are based on the physical interactions in the system and the environment. Emphasis has been placed on a design approach that systematically addresses modular forms of application development arising from well-planned system partitioning and containment. Many aspects have not been covered here. The references given at the end of this treatment will undoubtedly provide more detailed suggestions. Clearly, new problems will appear as applications achieve better performance metrics. Their solution must be based on critical thinking related to physics, rather than rote application of rules.

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